AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth below:

1. (Original) An apparatus, comprising:

- a driver to drive an output signal having a plurality of low-to-high (LH) and high-to-low (HL) signal transitions, with each of the signal transitions having a clock-to-output delay; and

- a pre-driver coupled to the driver, the pre-driver having a first and a second stage to cooperatively generate a reshaped waveform to trigger the LH and HL signal transitions of the output signal, with the first stage generating an initial waveform and the second stage modifying the initial waveform to generate the reshaped waveform based at least in part on a difference in the clock-to-output delays of the LH and HL signal transitions.

2. (Original) The apparatus according to claim 1, wherein the first stage is capable of setting a slew rate for the driver and the second stage is capable of changing the clock-to-output delay of one of the signal transitions of the output signal.

3. (Original) The apparatus according to claim 1, further comprising a compensator circuit coupled to the second stage to at least contribute to provision of a feedback in a form of a control signal, the control signal being capable of controlling an adjustment period during which the second stage modifies the initial waveform.

4. (Original) The apparatus according to claim 3, wherein the compensator circuit is capable of adaptively controlling the duration of the adjustment period to reduce the difference in the clock-to-output delays of the LH and HL signal transitions of the output signal.

5. (Original) The apparatus according to claim 3, further comprising a pre-driver control circuit coupled to the second stage and the compensator circuit to turn on the second stage in response to an input signal and to turn off the second stage in response to the control signal.

6. (Original) The apparatus according to claim 3, further comprising a voltage supply, coupled to the pre-driver and the compensator circuit, to provide a source voltage, having a voltage level, to the pre-driver and the compensator circuit; and wherein both the control signal and the difference in the clock-to-output delays of LH and HL signal transitions are in part a function of the source voltage level.

7. (Original) The apparatus according to claim 1, wherein the first stage, in response to an input signal, generates the initial waveform to trigger the LH signal transitions after a LH switching delay period and to trigger the HL signal transitions after a HL switching delay period; and a compensator circuit to generate a control signal having a feedback, wherein the feedback compensates for a time difference between the LH and HL switching delay periods.

8. (Original) The apparatus according to claim 7, wherein the second stage is responsive to the control signal to modify the initial waveform for an adjustment period occurring during at least a part of one of the switching delay periods to generate the reshaped waveform.

9. (Original) The apparatus according to claim 3, wherein the compensator circuit includes a pattern generator to generate a first and a second test signal with the second test signal being an inverted version of the first test signal; a first and a second test output buffer coupled to the pattern generator and responsive to the first and second test signals respectively to generate a first and a second test output signal respectively; a phase extraction circuit coupled to the first and second test output buffers to extract a phase difference between the first and second test output signals to generate the control signal.

10. (Original) The apparatus according to claim 9, further including a transition adjustment circuit coupled to the second stage to generate a pulse signal to control the adjustment period in response to the control signal; and wherein the phase extraction circuit and the transition adjustment circuit form a closed-loop feedback mechanism.

11. (Original) The apparatus according to claim 9, further comprising a pre-driver control circuit coupled to the second stage and the compensator circuit and having a first voltage control delay element responsive to an input signal to generate a signal to turn on the second stage and a second voltage control delay element responsive to the input signal and the control signal to generate a pulse signal to turn off the second stage.

12. (Original) The apparatus according to claim 11, wherein the control signal comprises a pair of bias voltages to delay the output of the pulse signal from the second voltage control delay element.

13. (Original) The apparatus according to claim 10, wherein the first and second test output buffers each include a test driver coupled to the phase extraction circuit to generate one of the test output signals; a test pre-driver coupled to the test driver with the test pre-driver having a first and a second test stage to cooperatively generate a test reshaped waveform to trigger the LH and HL signal transitions of one of the test output signals, with the first test stage generating a test initial waveform and the second test stage modifying the test initial waveform to generate the test reshaped waveform; and the control signal being capable of controlling the adjustment period during which the second test stage modifies the test initial waveform.

14. (Original) An apparatus, comprising:

- a driver to generate an output signal having a plurality of low-to-high (LH) and high-to-low (HL) signal transitions;

- a pre-driver having a first and a second stage commonly coupled to the driver and responsive to an input signal to generate a pre-driver waveform to trigger the LH signal

transitions after a LH switching delay period and to trigger the HL signal transitions after a HL switching delay period;

- a compensator circuit coupled to the driver to measure a quantity reflective of a difference between the LH and HL switching delay periods; and

- the second stage in communications with the compensator circuit to modify the pre-driver waveform during an adjustment period based upon the measured quantity, the adjustment period occurring during at least a portion of one of the switching delay periods.

15. (Original) The apparatus according to claim 14, the second stage is capable of adjusting the rate of voltage change of the pre-driver waveform during the adjustment period.

16. (Original) The apparatus according to claim 15, wherein the compensator circuit is capable of adaptively controlling the duration of the adjustment period to reduce a difference in the clock-to-output delays of the LH and HL signal transitions of the output signal.

17. (Original) The apparatus according to claim 14, further comprising a pre-driver control circuit coupled to the second stage and the compensator circuit, to turn on the second stage in response to an input signal and to turn off the second stage in response to the measured quantity.

18. (Original) The apparatus according to claim 17, wherein the pre-driver control circuit is capable of turning on the second stage during the LH or HL switching delay period which is longer; and the second stage is capable of increasing the rate of voltage change of the pre-driver waveform during the adjustment period.

19. (Original) The apparatus according to claim 18, wherein the pre-driver control circuit further including a first voltage control delay element, coupled to the second stage, to turn on the second stage in response to the input signal; and a second voltage control delay element, coupled to the second stage and the compensator circuit, to turn off the second stage in response to the measured quantity.

20. (Original) The apparatus according to claim 14, wherein the compensator circuit includes a pattern generator to generate a first and a second test signal with the second test signal being an inverted version of the first test signal; a first and a second test output buffer coupled to the pattern generator and responsive to the first and second test signals respectively to generate a first and a second test output signal respectively; a phase extraction circuit to extract a phase difference between the first and second test output signals to generate the measured quantity.

21. (Original) The apparatus according to claim 20, further comprising a transition adjustment circuit, coupled to the second stage and the compensator circuit, to generate a pulse signal to turn off the second stage in response to the measured quantity; and wherein the phase extraction circuit and the transition adjustment circuit form a closed-loop mechanism.

22. (Original) An apparatus, comprising:

- a pattern generator to generate a first and a second test signal with the second test signal being an inverted version of the first test signal;

- a first and a second weak pre-driver stage coupled to the pattern generator to generate a first and a second waveform respectively in response to the first and second test signals respectively, each of the waveforms having a plurality of low-to-high (HR) and a high-to-low (HL) switching delay periods;

- a first and a second driver coupled to the first and second weak pre-driver stages to generate a first and a second output signal respectively in response to the first and second waveforms respectively;

- a compensator circuit coupled to the first and second driver to generate a control signal on an output line in response to a phase difference between the first and second output signals; and

- a first and a second strong pre-driver stage coupled to the compensator circuit and responsive to the control signal to modify the waveforms during at least part of one of the switching delay periods to generate a modified waveform.

23. (Original) The apparatus according to claim 22, further comprising at least one bus output buffer connected to the output line to receive the control signal.

24. (Original) The apparatus according to claim 23, wherein the bus output buffer includes a bus weak pre-driver stage responsive to an input signal to generate a bus waveform, the bus waveform having a bus LH and a bus HL switching delay period; a bus strong pre-driver stage coupled to the output line and responsive to the control signal to modify the bus waveform for an adjustment period during at least one of the bus switching delay periods to generate a bus modified waveform; and a bus driver coupled to the bus weak and strong pre-driver stages to generate a bus output signal in response to the bus modified waveform.

25. (Original) The apparatus according to claim 22, further comprising a first and a second transition adjustment circuit coupled to the first and second strong pre-driver stages respective to generate a first and a second pulse signal to turn off the first and second strong pre-driver stages respectively in response to the control signal; and wherein the phase extraction circuit and the first and second transition adjustment circuits form a closed loop feedback mechanism.

26. (Original) The apparatus according to claim 25, wherein the phase extraction circuit includes a sampling circuit coupled to the first and second drivers to invert one of the first and second driver waveforms to generate an inverted signal and not to invert the other the driver waveform to generate a non inverted signal; and a phase detector for comparing the phase of the inverted and non-inverted signal to generate a difference signal.

27. (Original) The apparatus according to claim 26, wherein the phase extraction circuit further includes a low pass filter coupled to the phase detector to generate a filtered difference signal in response to the difference signal; and a bias voltage generator coupled to the low pass filter to generate at least one bias voltage in response to the filtered difference signal, the transition adjustment circuits each including a voltage control delay element coupled to the bias voltage generator to generate the pulse signal in response to the at least one bias voltage.

28. (Currently Amended) A system comprising

- a selected one of a graphics and a video controller;

- a bus coupled to the selected one of the graphic and video controller;

- a driver coupled to the bus to generate an output signal having a plurality of low-to-high (LH) and high-to-low (HL) signal transitions; [[~~and~~]] .

- an IC component having a pre-driver coupled to the driver, and having a first and a second stage responsive to an input signal to generate a pre-driver waveform to trigger the LH signal transitions after a LH switching delay period and to trigger the HL signal transitions after a HL switching delay period;

- a compensator circuit to extract a control signal representative of the time difference between the LH and HL switching delay periods; and

- a control circuit coupled to the compensator circuit and the second stage and responsive to the control signal to control an adjustment period during which the second stage is turned to reduce the time difference, the adjustment period including at least a portion of one of the switching delay periods.

29. (Cancelled)

30. (Currently Amended) The system according to claim [[~~29~~]]28, wherein the compensator circuit includes

- a pattern generator to generate a first and a second test signal with the second test signal being an inverted version of the first test signal; and

- a first and a second test output buffer coupled to the pattern generator and responsive to the first and second test signals respectively to generate a first and a second test output signal respectively; and

- a phase extraction circuit to extract a phase difference between the first and second test output signals to generate the control signal.

31. (Currently Amended) The system according to claim [[~~29~~]]28, wherein said control circuit is capable of turning on the second stage in response to an input signal and for turning off the second stage in response to the control signal.

32. (Currrently Amended) The system according to claim [[~~29~~]]28, further comprising a voltage supply, coupled to the pre-driver and the compensator circuit, to provide a source voltage, having a voltage level, to the pre-driver and the compensator circuit; and wherein both the control signal and the time difference in the clock-to-output delays of LH and HL signal transitions are in part a function of the source voltage level.

33. (Original) A method of operating an output buffer, comprising:

- generating an output signal of a driver having a plurality of low-to-high (LH) and high-to-low (HL) signal transitions;

- generating a pre-driver waveform for triggering the LH signal transitions after a LH switching delay period and for triggering the HL signal transitions after a HL switching delay period in response to an input signal;

- determining a difference between an LH clock-to-output delay for the LH signal transitions and a HL clock-to-output delay for the HL signal transitions; and

- compensating for the difference between the LH and HL clock-to-output delays by adjusting the rate of voltage change of the pre-driver waveform during at least part of one the switching delay periods.

34. (Currently Amended) The method according to claim [[31]]33, wherein compensating for the difference between the LH and HL clock-to-output delays includes increasing the rate of voltage change of the pre-driver waveform during at least part of one the switching delay periods.

35. (Currently Amended) The method according to claim [[31]]33, wherein compensating for the difference between the LH and HL clock-to-output delays includes adjusting the length of time during which the rate of voltage is changed.

36. (Currently Amended) The method according to claim [[31]]33, wherein compensating for the difference between the LH and HL clock-to-output delays includes increasing the rate of voltage change of the pre-driver waveform during at least part of the LH or HL switching delay period which is longer.

37. (Currently Amended) The method according to claim [[31]]33, wherein extracting the difference between an LH clock-to-output delay for the LH signal transitions and a HL clock-to-output delay for the HL signal transitions includes generating a first and a second test signal with the second test signal being an inverted version of the first test signal; driving a first and a second test output buffer with the first and second test signals respectively to generate a first and a second test output signal respectively; and extracting a phase difference between the first and second test output signals as representative of the difference between the LH and HL clock-to-output delays.